How to Resize Imager IP to Improve Productivity ?

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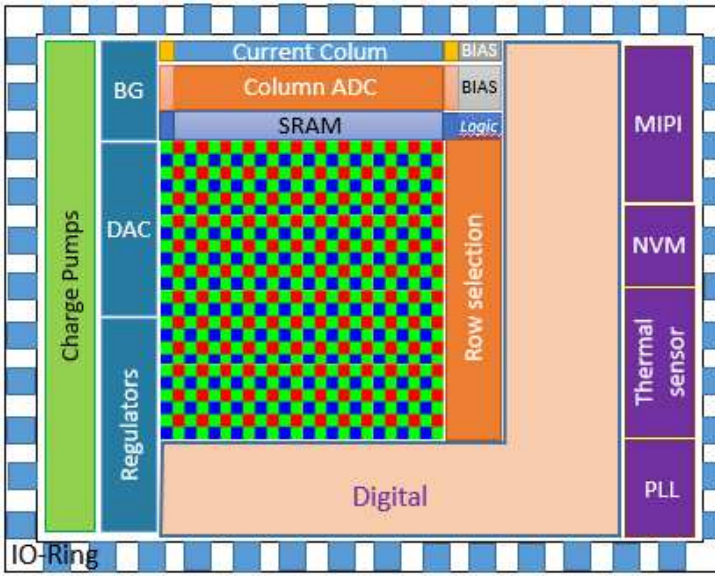
Contents

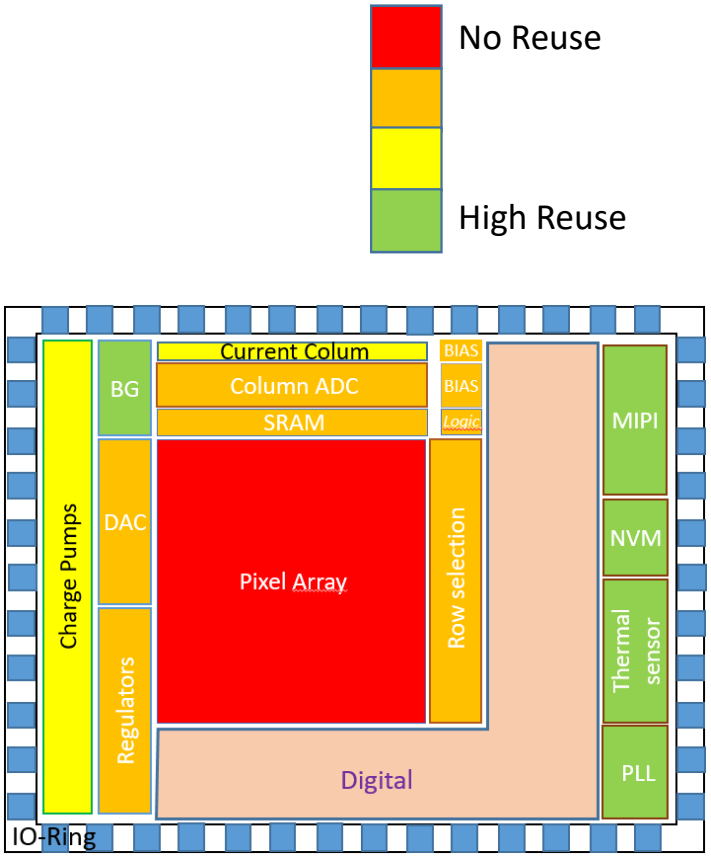
Analog IP blocks in image sensor

- Analog Peripheral (PLL, High Speed Serial links, Thermal sensor,…)
- Analog In-Column (Regulators, ADC/DAC, Charge Pump,…)
  - Regulators specification aligned with pixel array resolution
  - Charge pump links to regulators
  - Column ADC architecture could be the same, but pixel pitch different. So need fully re-layout and PVT post layout to do
  - DAC load and noise link to the number of columns
- Pixel
  - Several architecture and size according product specification
- Digital Part
  - Video-Timing Controller block
  - Bayer De-mosaic , Defect correction, …
- Non Volatile Memories
  - To Store the Firm-Ware.



Low Re-use blocks in image sensor

- Analog Peripheral: High Reuse
- Pixel : No Reuse
  - Few years ago: 1 process, 1 pixel, N products
  - Current trend: 1 product, 1 pixel, 1process
- Analog In-Column : Low Reuse
  - Same architecture, but column pitch different
  - Resizing activity
- Analog Drivers : Low reuse
  - Regulator Resizing due to different load

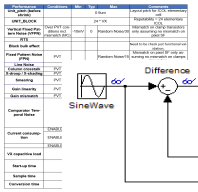


How to improve productivity ? (1) Methodology can help us

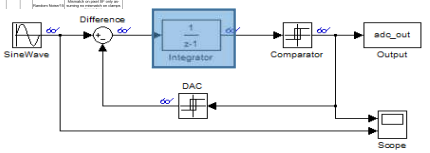
- Development Libraries under Management tools
  - Faster collaboration, Central db, better communication, share information,…
  - Methodics, ENOVIA Synchronicity
- Common simulation Flow/tools for every designer, every site
  - Reuse test-benches, better support, share expertize
- Top-Down approach
  - Top schematic early fully defined
  - Analog and Mix Simulation can start at the beginning of the development with analog models

How to improve productivity ? (2)
Disruptive Analog Design Team organization

- In the field of digital, the evolution of the tools, flows and ways of working have always evolved progressively to address the complexity
  - Modeling (Verilog, SystemVerilog, SystemC,…)
  - Team organization (architect, integration, verification)
- The Analog domain has become more and more complex, we have reached the frontier of changing the way of working to be more productive



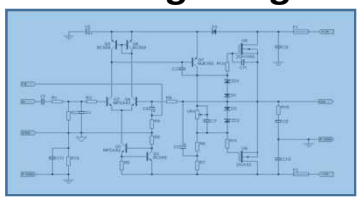
Analog Architect



Analog and Mix Validation

- SV models (Real Number)
- Spice netlist

Analog Designer

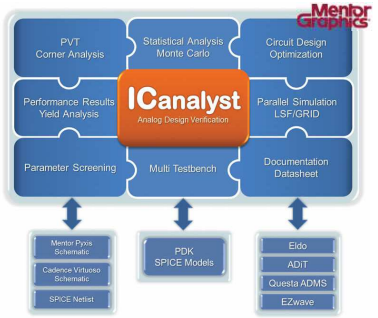


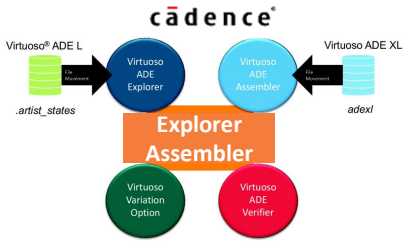
Analog Verifier

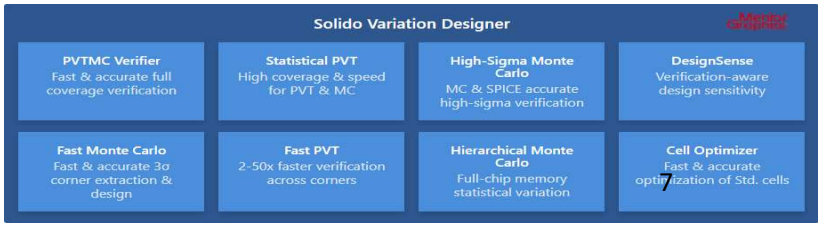
- PVT validation
- High-Sigma validation
- Optimization
- Resizing
- Migration

How to improve productivity ? (3)
What about tools ?

- Simulators to reduce Run Time, higher spice netlist, larger runs
  - Spice, FastSpice, Digital Fast Spice
- Run Time is not the only parameter
  - Tool integration in the flow is also important
- Analog Design Verification Cockpit
  - Classical method launching PVT and MC simulation for full verification including Multi test-benches
- More intelligent approach with Machine Learning to speed and increase the coverage
  - Solido Variation Manager (Fast PVT, Fast MC,…)

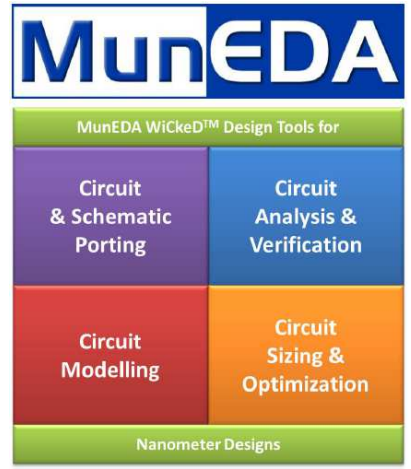






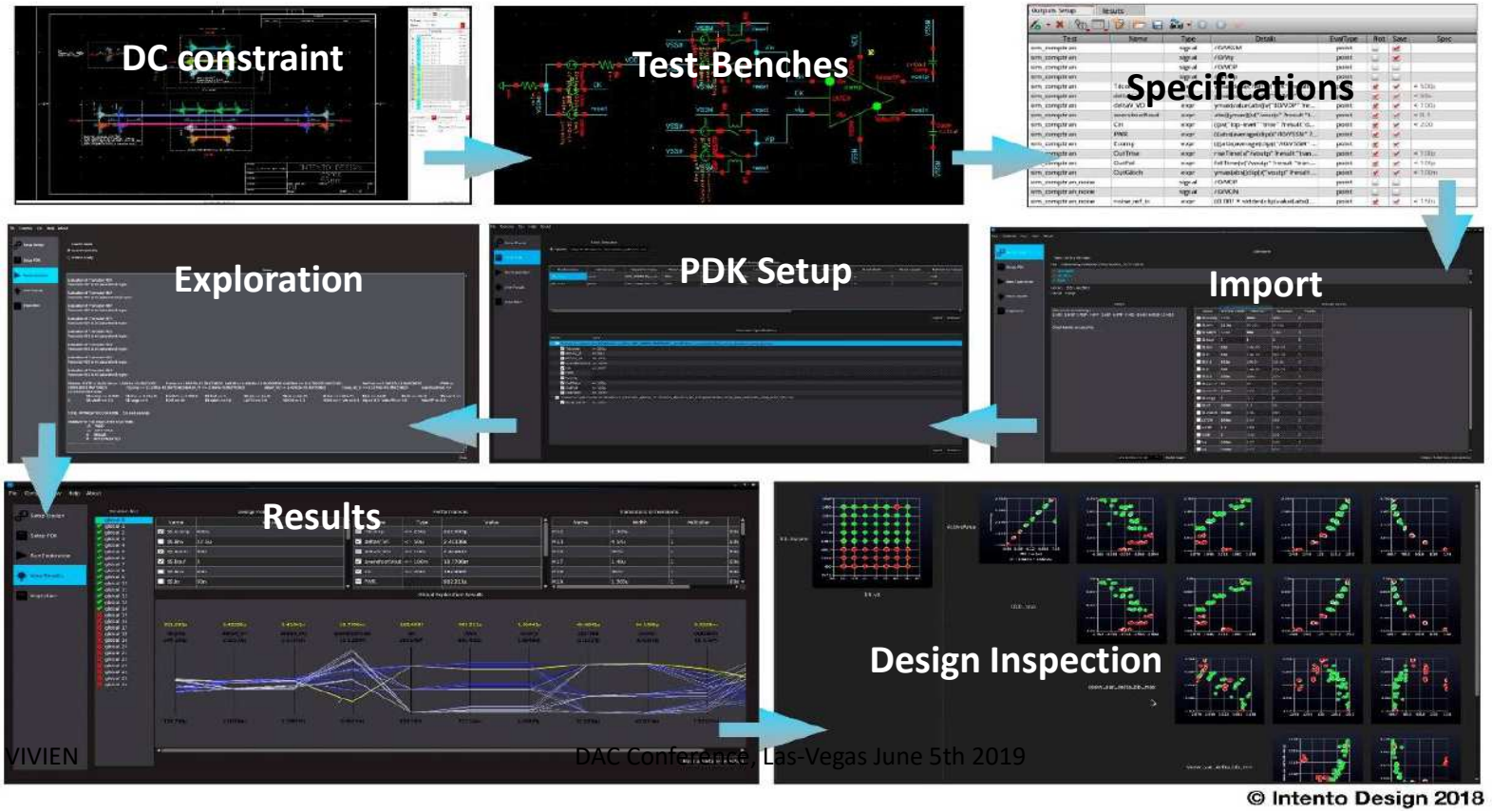
How to improve productivity ? (4)
What about tools ?

- Tools sizing and tuning (WiCkeD, MunEDA):
  - Optimization tools, to provide the best solution in PVT, MC based on specification
  - Faster Design, Better Performance, More Robust
- Design Exploration (IDxplore, INTENTO Design):
  - Provide Several Design Solutions to your Specifications



Design Exploration with Idxplore (1)

- IDxplore from INTENTO is a nice approach to provide several solutions and the final choice is done by the Designer.



Design Exploration with Idxplore (2)

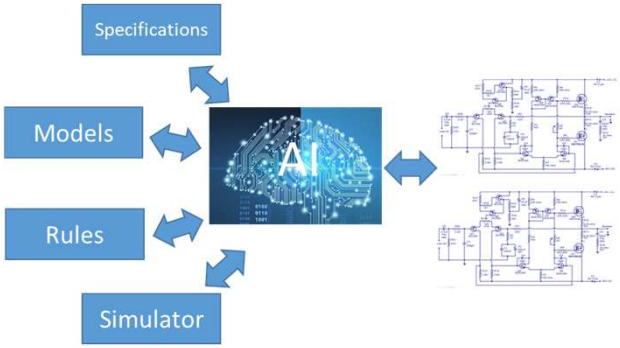
- IDxplore has been used to resize 10 Image Sensor regulators for smaller resolution
- Target
  - Same Noise, PSRR, Settling Time
  - But lower load and Less Power consumption
  - Size Reduction up to 20%
- Results
  - Classical method : 3 months
  - IDxplore : 4 weeks, including Explorer/Assembler Test-benches
    - All specifications reached and up to 50% of size reduction
    - Several solutions available (aggressive noise results, aggressive power consumption, aggressive area reduction)

Need more Disruptive approaches for analog blocks development (1)

- The past 30 years have seen an enormous growth in the power and sophistication of digital design tools, while progress in analog tools has been much more modest
- The Analog blocks architectures are more and more complex and the time to market is shorter and shorter
  - Modeling is used to validate the system complexity
  - But How to reduce the Design Blocks development ?
- For 20 years we have seen some solutions to size AOP
  - Interesting solution but limited to existing literature architecture
  - Is it the key for the future ?

Need more Disruptive approaches for analog blocks development (2)

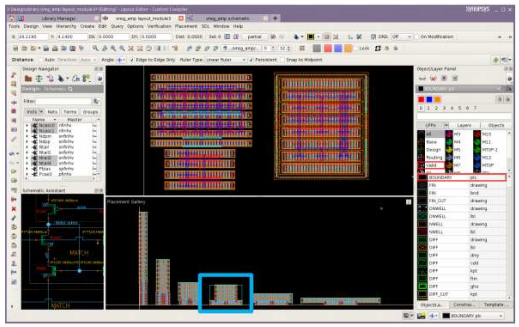
- The Artificial Intelligence could be the solution to develop Analog blocks
  - The hardware is progressing well
  - Machine learning is already in some tools to reduce verification time
- We have to invest more on AI for analog Development
  - Analog Design is comparable to a game with some rules

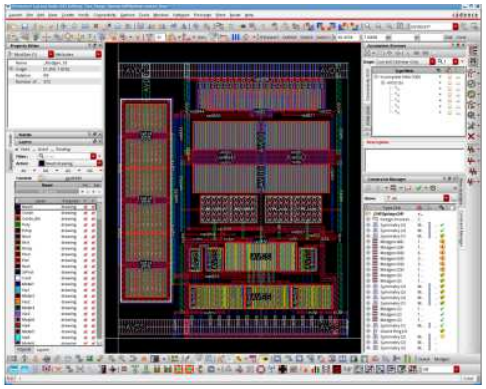


- The machine will be capable to be innovative with possible new design architecture never seen in the past

What about layout ? (1)

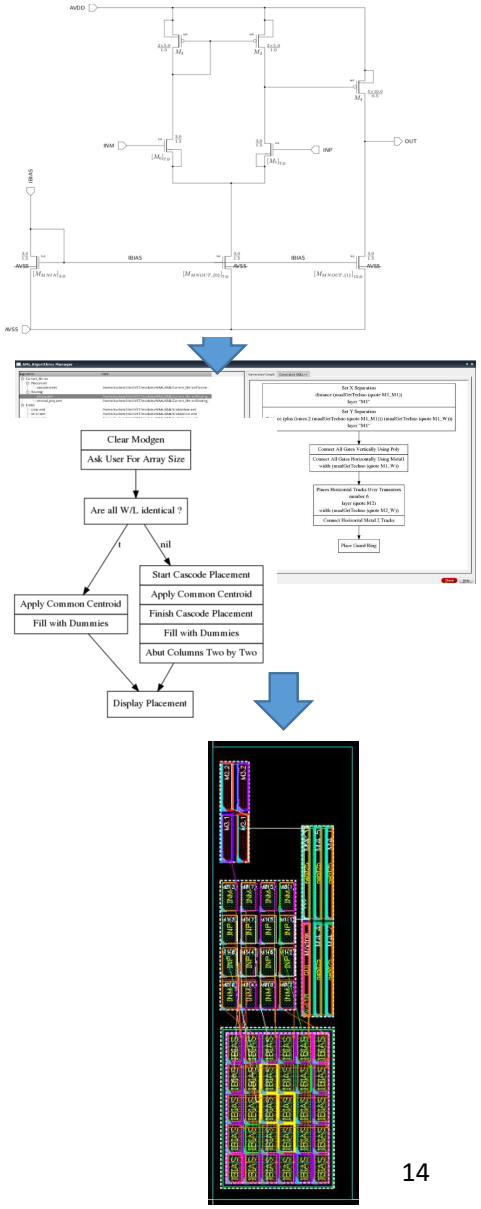
- Review of existing solution
  - Full custom algorithms
    - Time to capture the layout Designers needs
    - Huge Development Time
    - Heavy maintenance
  - Template
    - Huge number of templates to answer to all needs
    - Are the CAD vendors can address all the templates ?
  - Pcell
    - Development cost
    - Technology dependence





What about layout ? (2)

- Template with Machine Learning (ML) can help to find the right template or right algorithm, or combination of both
- Before ML can address this topic, we have to build basic bricks to build the algorithm
- In this way, algorithm can be easily understood and modified by the Analog Layout Designers and in this way they could better accept the automation



Conclusion

- Image sensor development needs huge effort for re-sizing analog blocks
- Methodology, the way of working can help us to be more productive
- Exploration tools from INTENTO design accelerate the development
- Nevertheless, we should have more Artificial Intelligence to go faster and to integrate more complexity

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Thank you for your attention!